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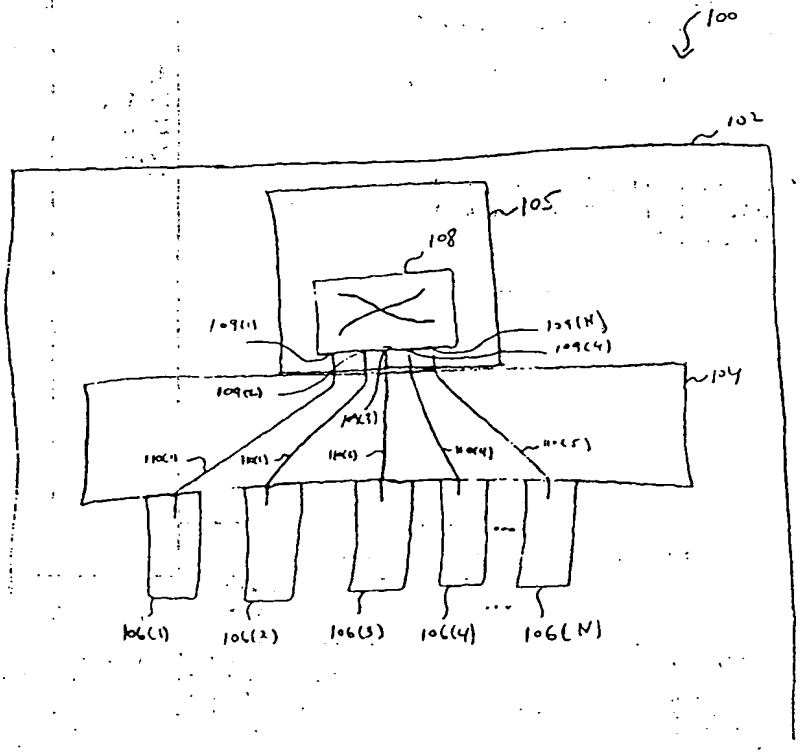
(54) Title: SYSTEM FOR INTERCONNECTING CIRCUIT BOARDS HOUSED WITHIN A CHASSIS

(57) Abstract

A computer system includes a chassis, a backplane housed within the chassis, a first board housed within the chassis and connected to the backplane, and a second circuit board housed within the chassis and connected to the backplane. The backplane includes a plurality of point–to–point data buses. The first circuit board includes a switching fabric having a plurality of data ports where one of the plurality of data ports is connected to one of the plurality of point–to–point data buses. The second circuit board includes a segmentation and reassembly (SAR) controller having a physical layer interface. The physical layer interface is connected to the point–to–point data bus that is connected to the switching fabric. In this manner, the second circuit board is interconnected to the first circuit board.



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System for Interconnecting Circuit Boards Housed Within a Chassis

Background of the Invention

Field of the Invention

The present invention relates generally to computer systems, and more specifically to a system for interconnecting circuit boards housed within a chassis.

Related Art

Practically every electronic computer system includes a chassis that houses a backplane and one or more circuit boards. The backplane is used to interconnect the one or more circuit boards, thereby enabling them to transmit data to each other. Each circuit board typically includes a microprocessor or other logic circuits for performing particular tasks.

Conventionally, the backplane includes at least one bus, and each circuit board within the chassis is connected to that bus. Thus, the bus is a shared resource. Data is transmitted over the bus from one board to another. There are a variety of buses that can be used, such as a time division multiplexed (TDM) bus or a packet bus.

Because a bus is shared by all the boards, only one board at any given time can transmit information onto the bus. This is one of several drawbacks of using a shared bus to interconnect circuit boards. Another drawback of the shard bus is that it typically experiences signal distortion and/or delay, and passive components are needed to terminate the bus. Additionally, a TDM bus, for example, suffers from a clock speed limitation because of the length of the bus. The clock speed is important because the clock speed of the bus determines the rate at which data can be transmitted between the circuit boards. Another

drawback of using a TDM bus is that all the circuit boards have to be synchronized.

Yet another disadvantages of using a shared bus to interconnect circuit boards is that data loss can easily occur if a new circuit board is added to the chassis and connected to the bus while one of the existing circuit boards is transmitting data onto the bus. Moreover, designing backplanes to overcome these disadvantages is time consuming and costly.

What is needed, therefore, is a system for interconnecting circuit boards housed within a chassis that cost effectively overcomes the above disadvantages.

Summary of the Invention

The present invention provides a computer system in which the circuit boards of the computer system are interconnected in a novel manner such as to overcome the above mentioned disadvantages of conventional computer systems. In one embodiment, the computer system includes a chassis, a backplane housed within the chassis, a first circuit board housed within the chassis and connected to the backplane, and a second circuit board housed within the chassis and connected to the backplane.

The backplane includes a plurality of point-to-point data buses. The first circuit board includes a switching fabric having a plurality of data ports where one of the plurality of data ports is connected to one of the plurality of point-to-point data buses. The second circuit board includes a segmentation and reassembly (SAR) controller having a universal test and operations physical layer interface for asynchronous transfer mode (ATM). The physical layer interface for ATM is directly connected to the point-to-point data bus that is connected to the switching fabric. In this manner, the second circuit board is interconnected to the first circuit board.

Brief Description of the Figures

The accompanying drawings, which are incorporated herein and form part of the specification, illustrate the present invention and, together with the description, further serve to explain the principles of the invention and to enable a person skilled in the pertinent art to make and use the invention. In the drawings, like reference numbers indicate identical or functionally similar elements. Additionally, the left-most digit(s) of a reference number identifies the drawing in which the reference number first appears.

FIG. 1 illustrates a computer system according to one embodiment of the present invention.

FIG. 2 illustrates passive backplane according to one embodiment.

FIG. 3 illustrates an exemplary SAR controller.

FIG. 4 further illustrates a master circuit board according to one embodiment.

FIG. 5 illustrates master circuit board 105 according to a second embodiment.

FIG. 6 further illustrates non-master circuit board 106(1). According to one embodiment.

Detailed Description of the Preferred Embodiments

FIG. 1 illustrates a computer system 100 according to one embodiment of the present invention. Computer system 100 includes a chassis 102 for housing a passive backplane 104, at least one master circuit board 105, and a number of non-master circuit boards 106(1)-106(N) (collectively 106). In one embodiment N is not greater than nine. However, one skilled in the art will recognize that the invention is not limited to any particular number of non-master circuit boards.

Master circuit board 105 and each non-master circuit board 106 are connected to backplane 104. Master circuit board 105 includes a switching fabric

108 having N ports 109(1)-109(N). Backplane 104 includes at least N point-to-point data buses 110(1)-110(N). Each data bus 110(1)-110(N) provides a point-to-point, full-duplex, data transmission path between one of the non-master circuit boards 106 and one of the ports 109 of switching fabric 108. For example, data bus 110(1) provides a point-to-point, full-duplex, data transmission path between circuit board 106(1) and port 109(1), data bus 110(2) provides a point-to-point, full-duplex, data transmission path between circuit board 106(2) and port 109(2), and data bus 110(N) provides a point-to-point, full-duplex, data transmission path between circuit board 106(N) and port 109(N). In one embodiment, data buses 110(1)-110(N) are all equal in length.

Further, in one embodiment, each data bus 110(1)-110(N) consists of 23 traces. A trace is a stip of conductor, such as copper, placed between ground planes. Preferably, each trace should have a constant impedance with no cross-talk characteristics and predictable dialectrics. In one embodiment, each trace has an impedance of 40 Ohms.

By providing a point-to-point, full-duplex, data transmission path between each non-master circuit board 106 and switching fabric 108, each board 106 is able to transmit data to any of the other boards. A board transmits data to another board (hereafter the "destination board") by transmitting packets or cells (depending on whether switching fabric is a packet switching fabric or a cell switching fabric) to fabric 108 over the data bus that connects the board to the fabric. The packet or cell includes an address portion and a data portion. The address portion contains an identifier that identifies the port 109 to which the destination board is connected.

For example, board 106(1) transmits data to board 106(N) by transmitting a packet or a cell to switching fabric 108, wherein the address portion of the packet or cell includes an identifier that identifies port 109(N). Upon receiving the packet or cell, switching fabric 108 examines the address portion to determine the port identified by the identifier contained therein. In this case, the identifier identifies port 109(N). The fabric then transmits the packet or cell out port

109(N) and onto data bus 110(N). The packet or cell is then received by board 106(N). Similarly, at the same time board 106(1) is transmitting data to board 106(N), board 106(2) can be transmitting information to board 106(1). Board 106(2) transmits data to board 106(1) by transmitting a packet or cell to switching fabric 108, wherein the address portion of the packet or cell contains an identifier that identifies port 110(1).

One advantage of this architecture is that the boards can transmit data to each other simultaneously, whereas in the conventional shared bus architecture only one board can transmit data onto the bus at any given time. Another advantage is that boards can be inserted into the chassis and connected to the fabric without disrupting another boards data transmission.

Backplane

FIG. 2 further illustrates passive backplane 104. According to one embodiment, backplane 104 includes connectors 201 and 202(1)-202(N). Connector 201 is used for physically connecting master circuit board 105 to backplane 104. Connectors 202(1)-202(N) are used for physically connecting non-master circuit boards 106(1)-106(N) to backplane 104.

Backplane 104 includes a power bus 204 that connects to an external power supply (not shown). When a non-master circuit board is attached to a connecter, and thereby connected to backplane 104, the circuit board receives power from power bus 204 through a power trace. For example, power trace 206(1) provides power to the circuit board connected to connector 202(1). Similarly, power traces 206(2)-206(N) provide power to the circuit boards connected to connectors 202(2)-202(N). Power trace 203 provides power to master circuit board 105. In one embodiment, power bus 204 is connected to a power supply that produces a voltage of -48 Volts.

In addition to including power traces 206(2)-206(N) and data buses 110(1)-110(N), backplane 104, in one embodiment, also includes power on/off data buses 210(1)-210(N) and utility data buses 212(1)-212(N). Power on/off

data buses 210(1)-210(N) are used to activate or deactivate the circuit boards connected to connectors 202(1)-202(N), respectively. Utility data buses 212(1)-212(N) are used for, among other things, transmitting circuit board characteristics to master circuit board 105.

Exemplary Master Circuit Board

FIG. 4 further illustrates master circuit board 105 according to one embodiment. As illustrated in FIG. 4, master circuit board 105 includes a management system 402 in addition to switching fabric 108. It is not a requirement that management system 402 be on the same circuit board as switching fabric 108. Thus, it is contemplated that there could be other embodiments where management system 402 and switching fabric 108 are placed on separate circuit boards.

There is also provided a power converter 403, which is connected to power trace 203 when board 105 is connected to backplane 104. Power converter 403 converts the voltage supplied by power bus 204 to the voltage necessary to power management system 402 and switching fabric 108.

In one embodiment, switching fabric 108 is an asynchronous transfer mode (ATM) switching fabric. In an alternative embodiment, switching fabric 108 is an Ethernet switching fabric. One skilled in the art will recognize that a variety of switching fabrics could be used, provided the switching fabric has, among other things, adequate throughput. Preferably, the switching fabric is a 5 Gigabit memory based ATM switching fabric, such as the ATMS1040 switching fabric sold by MMC Networks, Inc.

In one embodiment, management system 402 is responsible for, among other things, monitoring the non-master circuit boards connected to backplane 104 and activating/deactivating those circuit boards. Circuit boards are connected to backplane 104 in a powered off (i.e., deactivated) state to reduce the chance of arcing. Management system 402 can power on (i.e. activate) a circuit board

connected to backplane 104 by sending a signal through the power on/off data bus that connects management system 402 to that circuit board.

Management system 402 is programmed such that before activating a circuit board 106 manager system 402 first determines the power requirements of the board 106 and the available power. Management system 402 determines power requirements of a board by transmitting a predetermined signal to the board through the utility data bus that connects the management system 402 to the board. In response to receiving the predetermined query, the board transmits its power requirements to manager system 104. If the power requirements of the board are less than or equal to the available power, manager system 104 activates the board by transmitting a predetermined signal over the power on/off data bus that connects manager system 104 with the board.

In one embodiment, Management system 402 includes a processing unit 490 that includes a microprocessor 480, a chipset 481, and a memory 492 for storing data and program instructions that control microprocessor 480. There is also included an input/output system 491 for enabling processing unit 490 to communicate and control (e.g., activate and deactivate) the circuit boards connected to backplane 104. Input/output system 491 is connected to power on/off data buses 210(1)-210(N) and utility data buses 212(1)-212(N) when board 105 is connected to backplane 104. A bus 496 couples input/output system 491 with processing unit 490. Preferably, bus 496 is a 32-bit peripheral component interconnect (PCI) bus with Universal I/O.

Management system 402 also includes a segmentation and reassembly (SAR controller) controller 494 that is directly connected to a data port of switching fabric 108 and to bus 496. Referring now to FIG. 3, a top-level diagram of the general architecture of SAR controller 494 is illustrated. SAR controller 494 has segmentation and reassembly engines 306 and two interfaces: a bus interface 302 and a UTOPIA interface 304. UTOPIA interface 304 is a physical layer interface. Perferably, UTOPIA interface 304 implements the industry standard Universal Test and Operations Physical Layer Interface for

ATM (UTOPIA). Bus interface 302 interfaces SAR controller to bus 496, and therefore couples SAR controller 494 to processing unit 490. Preferably, bus interface is a PCI bus interface with a 32-bit wide data bus. In one embodiment, SAR controller 494 masters bus 496 in its master mode and allows processing unit to access SAR controller 494 in slave-mode operation.

UTOPIA interface 304 of SAR controller 494 is directly connected to a port of switching fabric 108. Because UTOPIA interface 304 of SAR controller 494 is connected to a port of switching fabric 108 and because SAR controller can receive data from management system 402 through bus 496, management system 402 is able to transmit data through switching fabric 108 to any circuit board connected to backplane 104. To transmit data from management system 402 to a circuit board connected to backplane 104, management system 402 transmits data to SAR controller 494 using bus 496. Upon receiving the data, SAR controller creates a cell 484 and transmits the cell 484 to switching matrix 108. Cell 484 consists of a data segment and a header segment. Contained in the data segment is the data or a portion of the data transmitted to SAR controller 494 from management system 402. Contained in the header segment is, among other things, information that identifies the port of switching fabric 108 to which the destination board (i.e., the board to which the data is to be transmitted) is connected. Upon receiving cell 484, switching matrix 108 examines the header segment to determine the port to which the destination board is connected, and transmits the cell to that board using the data bus 110 that connects that board to switching fabric 108.

FIG. 5 illustrates master circuit board 105 according to a second embodiment. The second embodiment of circuit board 105 is like the embodiment shown if FIG. 4 with the exception that a router 502 has been added thereto. Router 502 connects to an external network 530 through a network interface 522. Network 530 can be a local area network (LAN) or a wide area network (WAN), for example. Router 502 includes a microprocessor 510 interfaced to a chipset 512. Chipset 512 is interfaced to a main memory 514 and

a bus 516. Also interfaced to bus 516 is a packet memory 520 and a SAR controller 518. SAR controller 518 is further interfaced with switching fabric 108 in the same manner as SAR controller 494. FIG. 3 illustrates a top-level diagram of SAR controller 518.

Router 520 can route data 532 from network 530 to any circuit board connected to backplane 104. Data 532 is received from network 530 by network interface 522 and stored in packet memory 520. SAR controller 518 creates one or more cells from data 532 and transmits the cells to switching fabric, which then switches the cells to a circuit board connected to backplane 104. Router 502 is further disclosed in U.S. Patent Application No. 09/244,971, (Attorney docket number 1698.0090000), filed February 10, 1999, entitled "System And Method For Reducing Memory Contention in a Data Processing Device," which is assigned to the assignee of the present invention, and incorporated herein by reference.

Exemplary non-master circuit board

FIG. 6 further illustrates non-master circuit board 106(1). According to one embodiment, circuit board 106(1) includes a microprocessor 610 interfaced with a chipset 612. Chipset 612 is interfaced with a main memory 620 and a bus 604. Also interfaced with bus 604 is a memory 606 and a SAR controller 602, which is further illustrated in FIG. 3. SAR controller 602 includes a segmentation/reassembly engine 306, a bus interface 302, and a UTOPIA interface 304, all of which are described above. Preferably, bus 604 is a peripheral component interconnect (PCI) bus, and chipset 612 and SAR controller 602 are PCI bus masters.

When circuit board 106(1) is connected to backplane 104, UTOPIA interface 304 of SAR controller 602 is directly connected to data bus 110(1) through signal lines 601. Therefore, when circuit board 106(1) and master circuit board 105 are connected to backplane 104, SAR controller 602 is directly coupled to a port of switching fabric 108.

Circuit board 106(1) also includes a power converter 640, which is connected to power trace 206(1) when board 106(1) is connected to backplane 104. Power converter 640 converts the voltage supplied by power bus 204 to the voltage necessary to power the various components on circuit board 106(1).

In one embodiment, data from circuit board 106(1) that is to be transmitted to one of the other circuit boards 106(2)-(N) or master circuit board 105 is stored in one of the buffers 608(1)-(X) of memory 606. Other configurations of memory 606 are contemplated. The function of SAR controller 602 is to transmit the data stored in buffers 608(1)-(X) to switching fabric 108. SAR controller 602 accomplishes this by retrieving a fixed amount of data from one of the buffers, adding a header to the fixed amount of data, thereby creating a cell, and transmitting the cell directly onto data bus 110(1), where it is then received at port 109(1) of switching fabric 108.

The header that SAR controller 602 adds to the fixed amount of data contains, among other things, information used by switching fabric 108 to identify the port to which the cell should be switched. In one embodiment, the information includes a virtual path identifier (VPI) and a virtual circuit identifier (VCI). Each buffer 608 is associated with a VPI/VCI pair. Therefore, when SAR controller 602 creates a cell by adding a header to data taken from one of the buffers 608(1)-(X), the VPI/VCI that is placed in the header of the cell is the VPI/VCI that is associated with the buffer from which the data was taken. Thus, each buffer is associated with one of the other circuit boards in the system. Consequently, when microprocessor 610 has data that must be transmitted to a circuit board connected to backplane 104, microprocessor 610 directs chipset 612 to store the data in the buffer associated with that circuit board. SAR controller 602 is then responsible for transmitting the data to switching fabric 108.

Circuit board 106(1) may also include a network interface 630 that is interfaced to bus 604. Network interface 630 can be a LAN network interface, WAN network interface, or other type of network interface. When network interface 630 receives data from the network to which it is connected, it stores

that data in memory 606 using bus 604. Next, microprocessor 610 determines the circuit board 106(2)-(N) to which the data should be routed based on a forwarding table (not shown) stored in main memory 620. In one embodiment, the forwarding table is created by management system 402 and distributed by management system 402 to each circuit board 106(1)-(N) connected to backplane 104.

After determining the circuit board 106(2)-(N) to which the data should be routed, microprocessor 610 directs chipset 612 to move the data to the buffer 608(1)-(X) associated with that circuit board. As described above, SAR controller 602 transmits the data to switching fabric 108 by creating cells containing the data and transmitting those cells to switching fabric 108.

According to one embodiment, circuit board 106(1) also includes a memory 642 for storing information relating to the characteristics of circuit board 106(1) and a temperature sensor 644 for measuring the temperature of circuit board 106(1). Temperature sensor 644 stores temperature measurement readings in memory 642. Preferably, memory 642 is an electronically erasable programmable read only memory (EEPROM), however, other memory devices are contemplated, such as a programmable read only memory (PROM), erasable PROM, flash memory, or the like. When circuit board 106(1) is connected to backplane 104, memory 642 is connected to utility data bus 212(1), which is connected to management system 402. This gives management system 402 access to the contents of memory 642, thereby enabling management system 402 to determine the characteristics of circuit board 106(1), including its temperature and power requirements. As described above, management system 402 will not activate circuit board 106(1) if its power requirements exceed the available power. Management system 402 activates circuit board 106(1) by transmitting a predetermined signal to power converter 640 using power on/off data bus 210(1).

Conclusion

While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example, and not limitation. It will be understood by those skilled in the relevant art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the following claims. Thus the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

What Is Claimed Is:

1. A computer system, comprising:

a chassis;

a backplane housed within said chassis, said backplane comprising a plurality of point-to-point data buses;

a first circuit board housed within said chassis and connected to said backplane, said first circuit board comprising a switching fabric having a plurality of data ports, one of said plurality of data ports being connected to one of said plurality of point-to-point data buses;

a second circuit board connected to said backplane, said second circuit board comprising a SAR controller having a physical layer interface, said physical layer interface being directly connected to said one of said plurality of point-to-point data buses, thereby enabling said SAR controller to transmit cells to said switching fabric.

2. The computer system of claim 1, wherein said physical layer interface is a Universal Test and Operations Physical Layer Interface for ATM.

3. The computer system of claim 1, wherein said first circuit board further comprises a management system, said management system comprising a second SAR controller that is connected to one of said plurality of data ports.

4. The computer system of claim 3, wherein said second SAR controller comprises a second physical layer interface, said second physical layer interface being directly connected to said one of said plurality of data ports.

5. The computer system of claim 4, wherein said second physical layer interface is a Universal Test and Operations Physical Layer Interface for ATM.

6. The computer system of claim 1, wherein each of said plurality of point-to-point data buses comprises a plurality of traces.

7. The computer system of claim 1, wherein each of said plurality of point-to-point data buses comprises at least twenty-three traces.

8. A circuit board, comprising:

a switching fabric having a plurality of data ports for receiving cells; and

a management system comprising a bus, a processing unit, and a SAR controller, said processing unit and said SAR controller being interfaced to said bus, said SAR controller comprising a physical layer interface that is directly connected to one of said data ports.

9. The circuit board of claim 8, wherein said physical layer interface is a Universal Test and Operations Physical Layer Interface for ATM.

10. The circuit board of claim 8, wherein said bus is a PCI bus.

11. The circuit board of claim 8, further comprising a router comprising a network interface for interfacing to a network, a bus, and a second SAR controller, said network interface and said second SAR controller being interfaced to said bus, and said second SAR controller having a second physical layer interface that is directly connected to one of said data ports.

12. The circuit board of claim 11, wherein said second physical layer interface is a Universal Test and Operations Physical Layer Interface for ATM.

13. A circuit board adapted to connect to a backplane comprising a plurality of point-to-point data buses, comprising:

a bus;

a processing unit interfaced to said bus; and

a SAR controller comprising a bus interface for interfacing said SAR controller to said bus and comprising a physical layer interface,

wherein when the circuit board is connected to the backplane said physical layer interface is directly connected to one of the plurality of point-to-point data buses.

14. The circuit board of claim 13, wherein said physical layer interface is a Universal Test and Operations Physical Layer Interface for ATM.

15. The circuit board of claim 13, further comprising a network interface system for interfacing the circuit board to a network, said network interface system being interfaced to said bus.

16. A computer system, comprising:

a chassis;

a backplane housed within said chassis, said backplane comprising:

a first circuit board connector;

a plurality of second circuit board connectors;

a first set of point-to-point data buses;

a second set of point-to-point data buses; and

a third set of point-to-point data buses,

wherein the number point-to-point data buses within said first set of point-to-point data buses, within said second set of point-to-point data buses, and within said third set of point-to-point data buses is equal to the number of second circuit board connectors, and wherein each point-to-point data bus within said first set of point-to-point data buses connects one of said plurality of second circuit board connectors to said first circuit board connector, each point-to-point data bus within said second set of

point-to-point data buses connects one of said plurality of second circuit board connectors to said first circuit board connector, and each point-to-point data bus within said third set of point-to-point data buses connects one of said plurality of second circuit board connectors to said first circuit board connector; and

a first circuit board adapted to connect to said first circuit board connector, said first circuit board comprising a switching fabric and a management system, said switching fabric comprising a plurality of data ports,

wherein when said first circuit board is connected to said first circuit board connector each point-to-point data bus within said first set of point-to-point data buses is interfaced to a unique on of said plurality of data ports, and each point-to-point data bus within said second and third set of point-to-point data buses is interfaced to said management system.

17. The computer system of claim 16, wherein said switching fabric is an asynchronous transfer mode (ATM) switching fabric.

18. The computer system of claim 17, wherein said ATM switching fabric is a memory based ATM switching fabric.

19. The computer system of claim 18, wherein said ATM switching fabric is at least a five gigabit switching fabric.

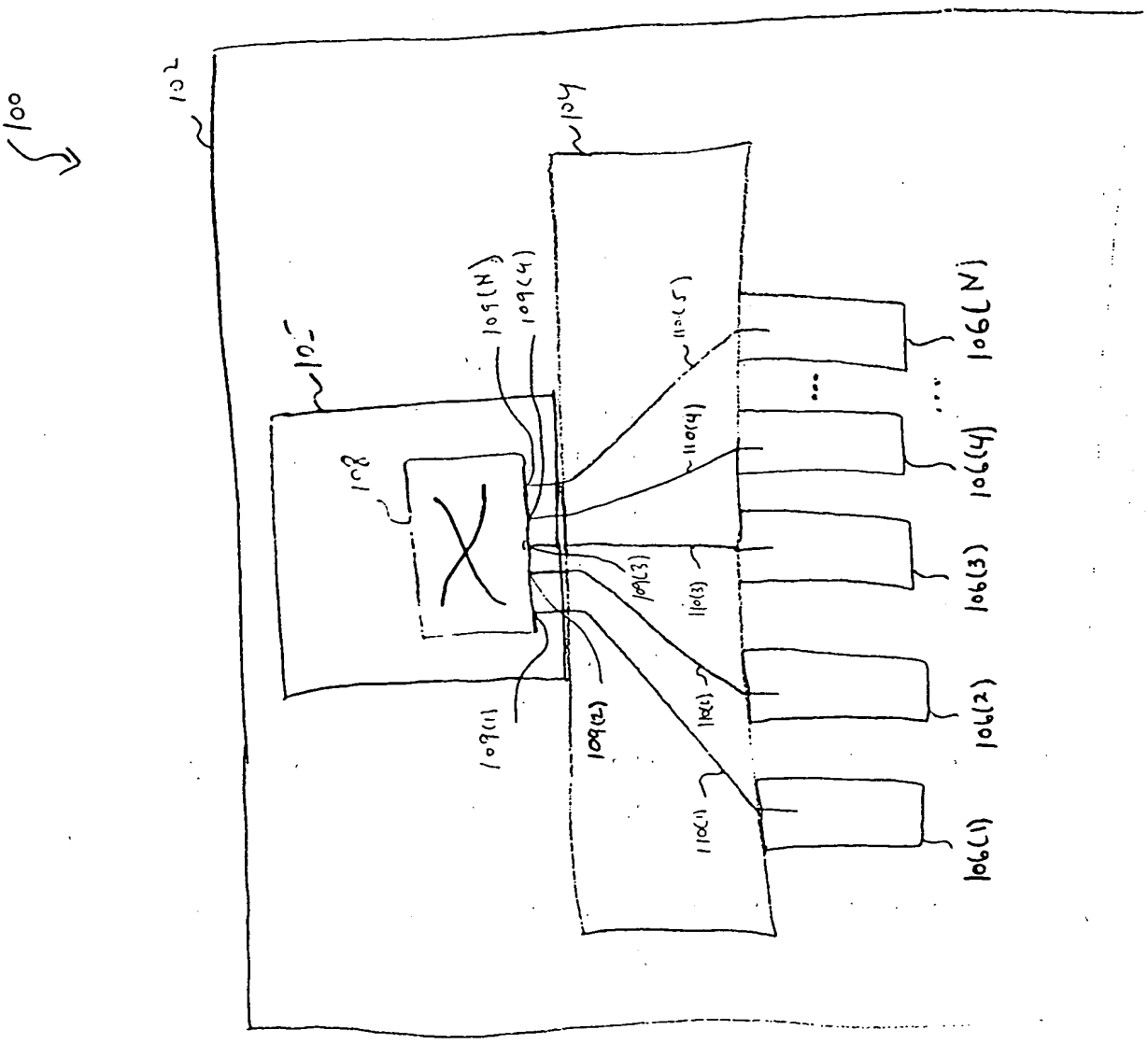
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FIG. 1

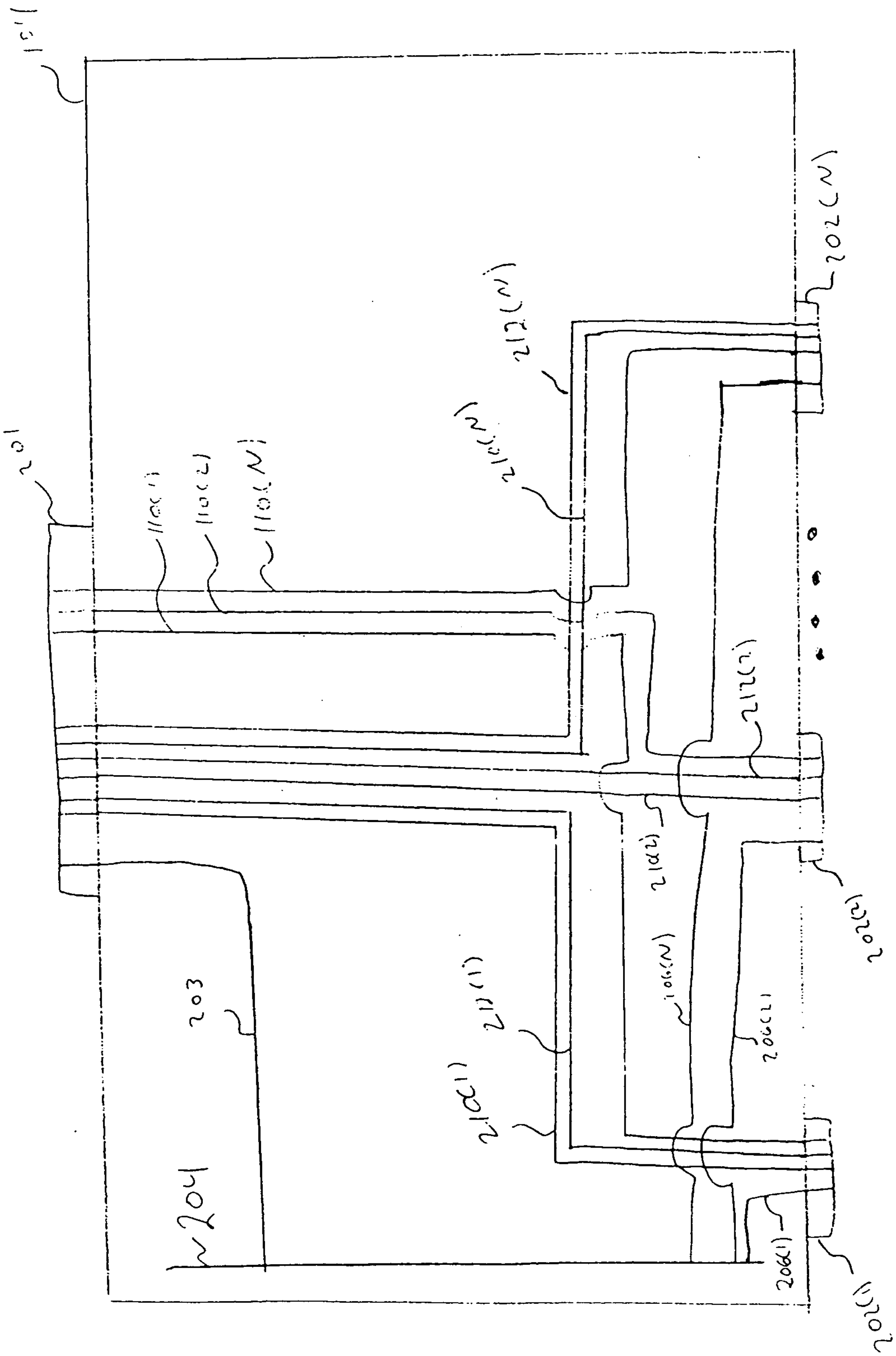
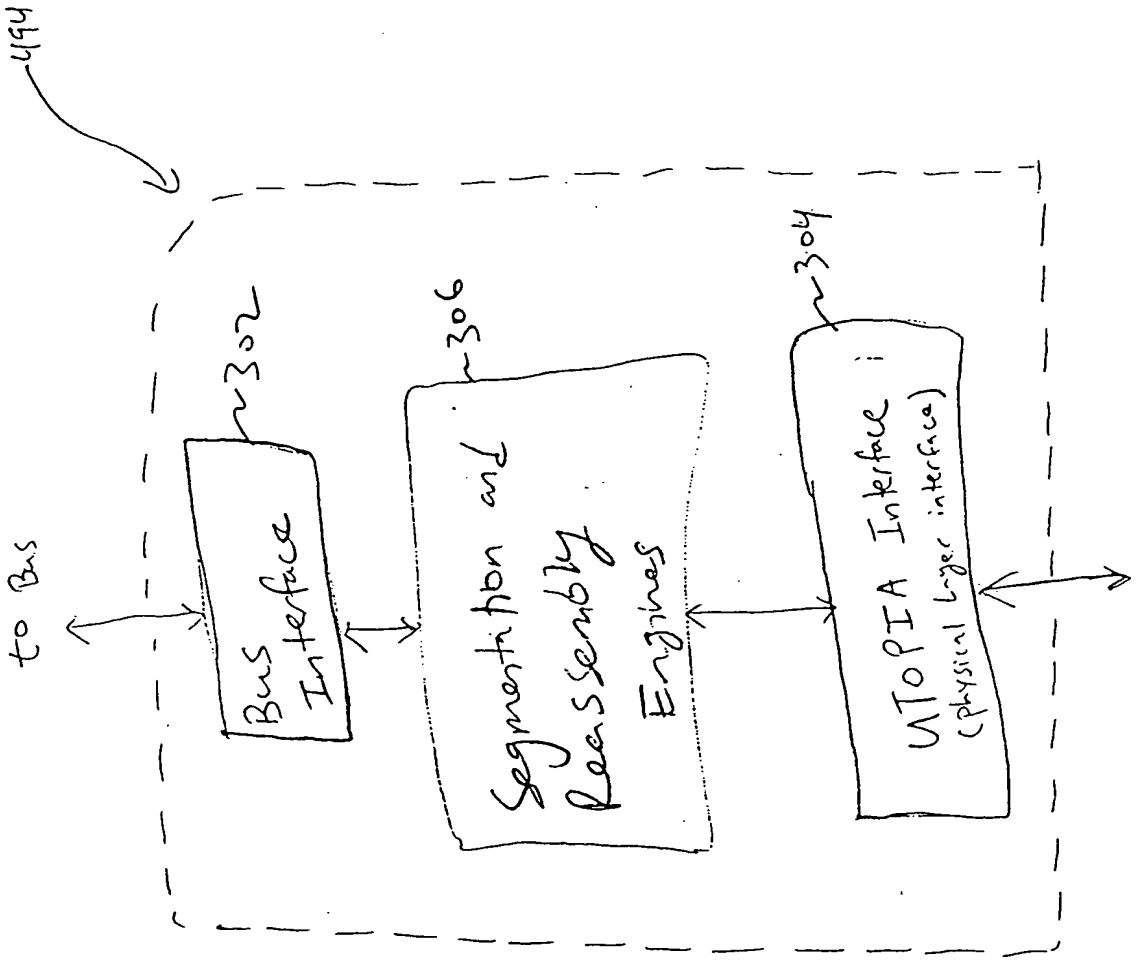


FIG 2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Bus Interface
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Segmentation and Reassembly Engines
306
UTOPIA Interface
(Physical Layer interface)
304

FIG. 3

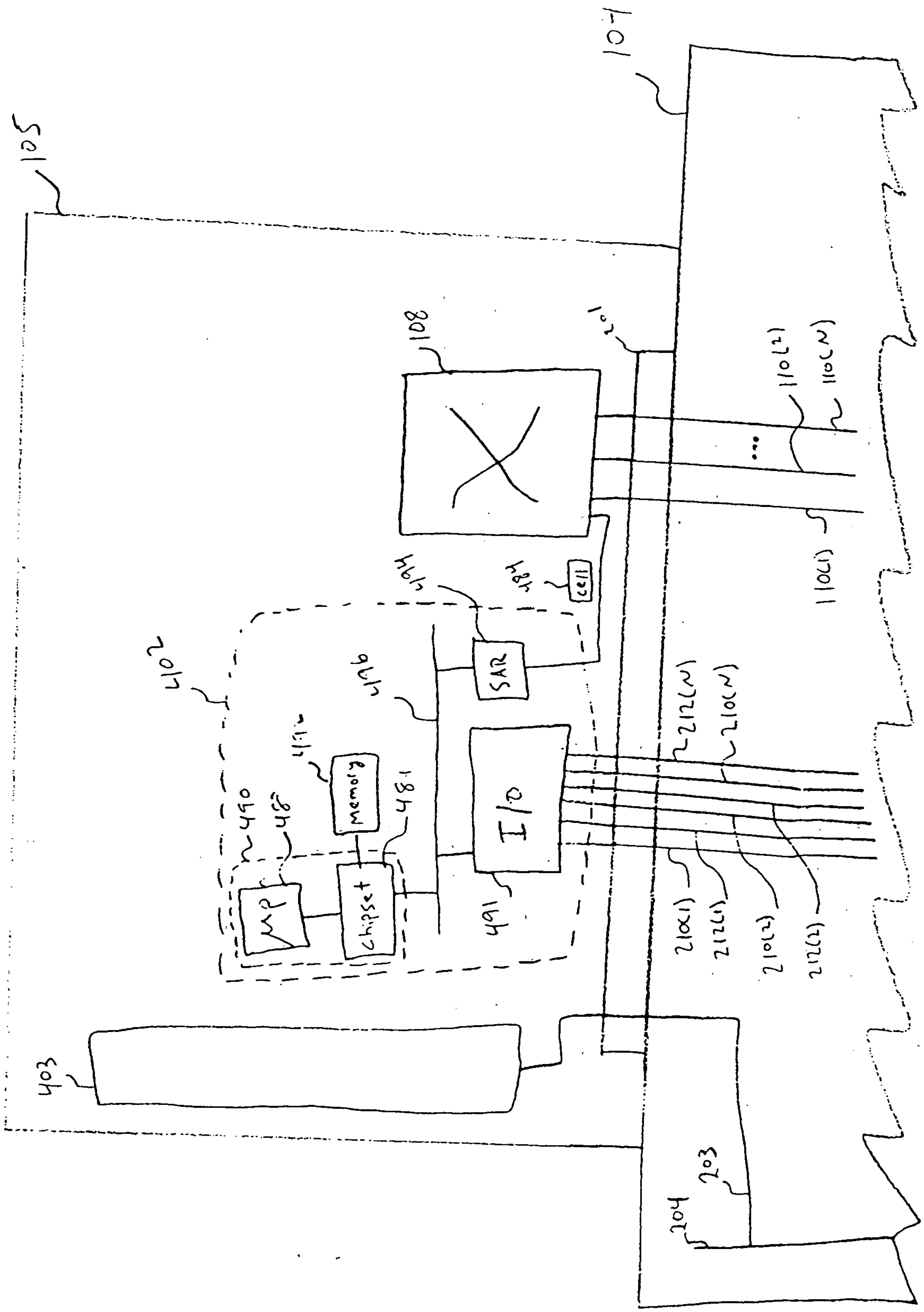
101
105
108
201
110(1)
110(2)
110(N)
494
487
Cell
SAR
496
402
472
Memory
490
488
481
MP
Chipset
I/O
491
212(N)
210(N)
210(1)
212(1)
210(2)
212(2)
403
203
204

FIG 4

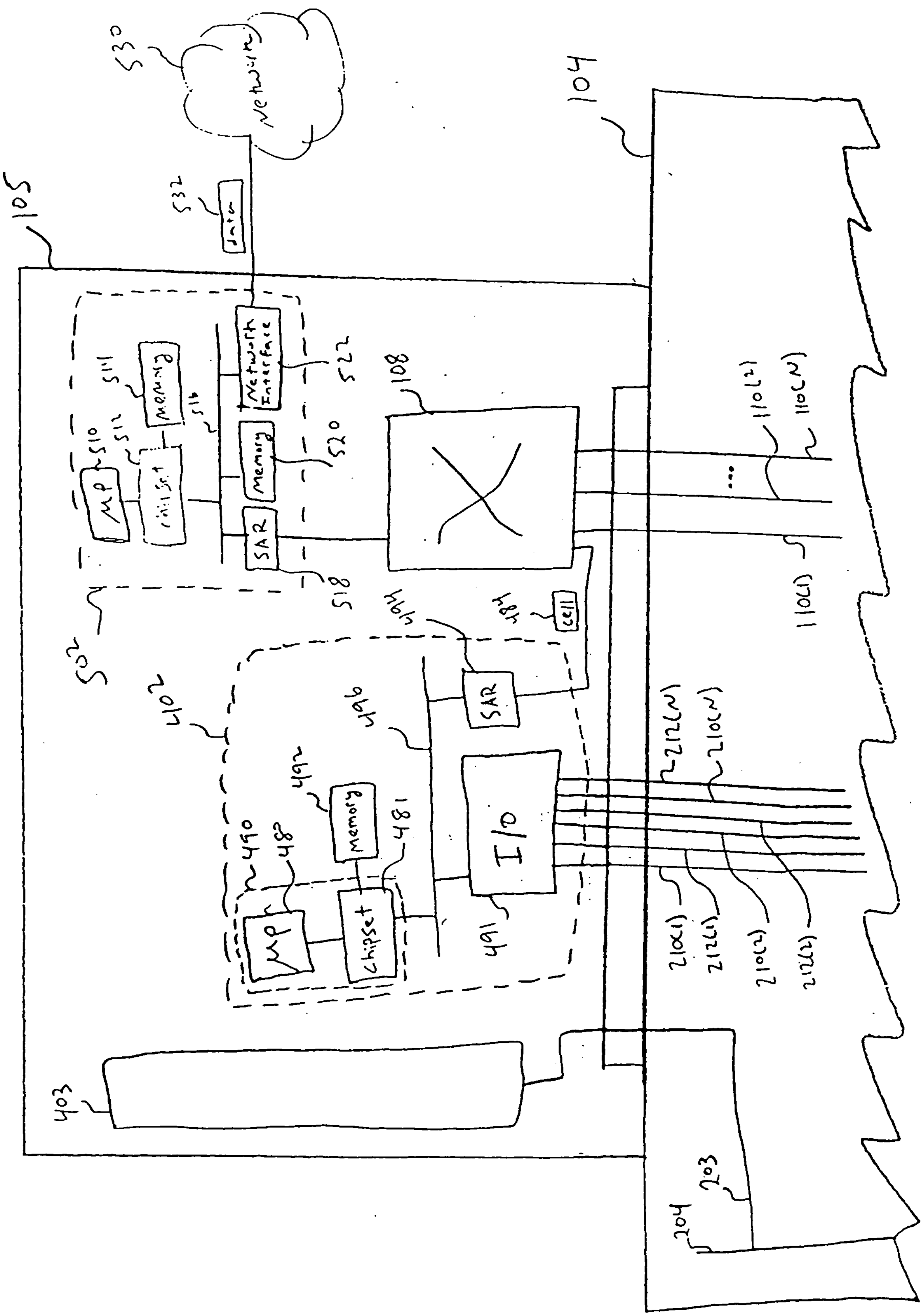
Network
Network Interface
Memory
SAR
MP
Chipset
I/O
cell
530
532
105
104
108
502
510
520
522
518
402
403
490
492
494
496
481
491
203
204

FIG. 5

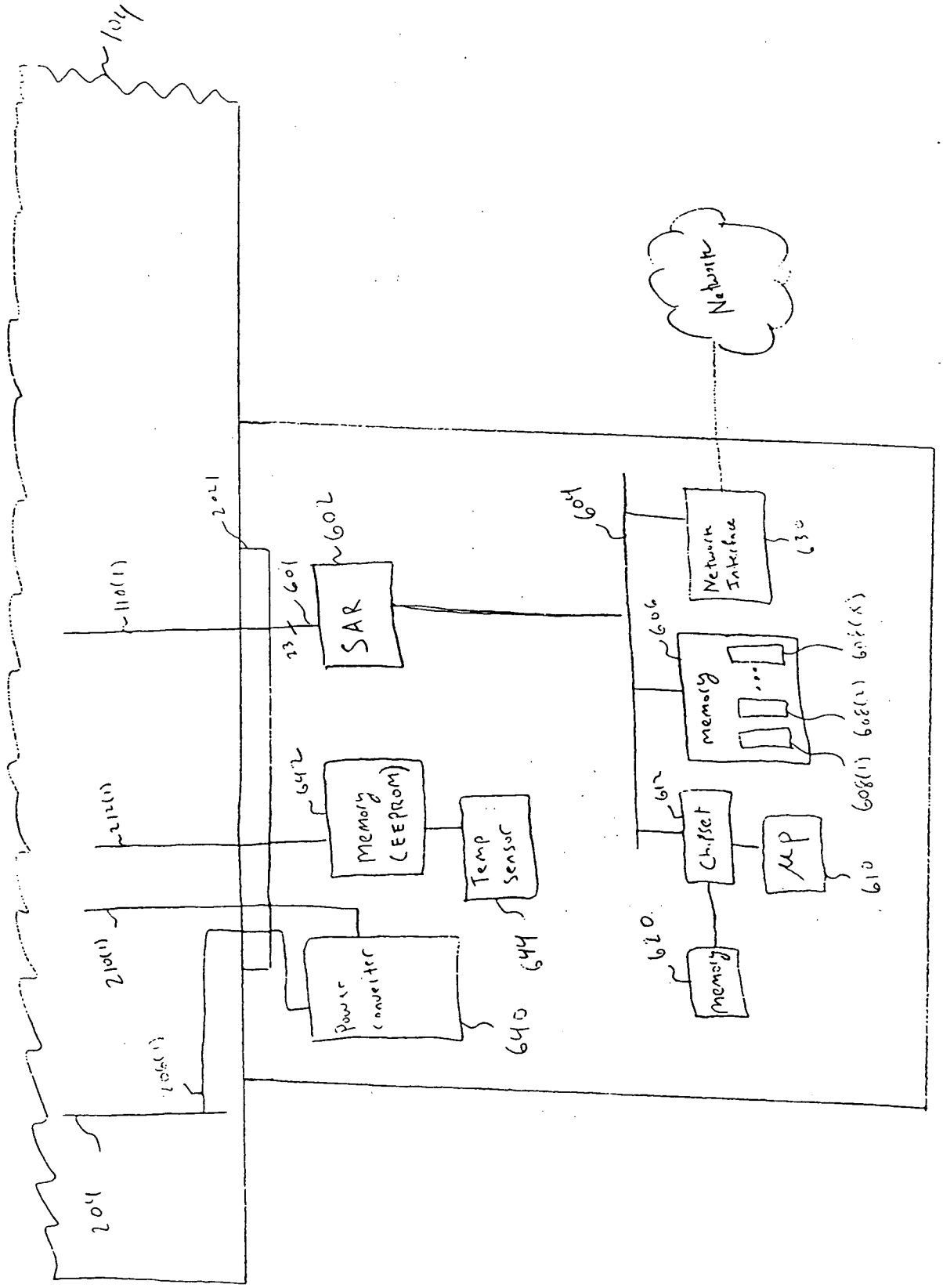
104
Network
SAR
602
601
603
Network Interface
630
606
memory
610
608(1)
608(N)
Chipset
616
μP
620
memory
Memory (EEPROM)
642
Temp Sensor
644
Power converter
640
110(1)
112(1)
114(1)
116(1)
118(1)
201

FIG. 6

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(74) Agents: SOKOHL, Robert, E. et al.; Sterne, Kessler, Goldstein & Fox P.L.L.C., Suite 600, 1100 New York Avenue, N.W., Washington, D.C. 20005-3934 (US).

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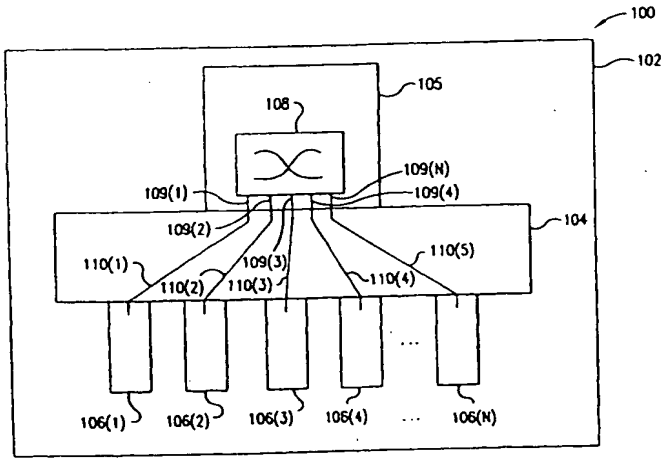
Published:
— *With international search report.*

(88) Date of publication of the international search report:
4 January 2001

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SYSTEM FOR INTERCONNECTING CIRCUIT BOARDS HOUSED WITHIN A CHASSIS



(57) Abstract: A computer system includes a chassis, a backplane housed within the chassis, a first board housed within the chassis and connected to the backplane, and a second circuit board housed within the chassis and connected to the backplane. The backplane includes a plurality of point-to-point data buses. The first circuit board includes a switching fabric having a plurality of data ports where one of the plurality of data ports is connected to one of the plurality of point-to-point data buses. The second circuit board includes a segmentation and reassembly (SAR) controller having a physical layer interface. The physical layer interface is connected to the point-to-point data bus that is connected to the switching fabric. In this manner, the second circuit board is interconnected to the first circuit board.

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/06586

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F13/40 H04Q11/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 742 765 A (GHUFRAN SALMAN ET AL) 21 April 1998 (1998-04-21)	1,16
A	column 1, line 40 -column 2, line 32 column 3, line 3 -column 4, line 13 column 6, line 9 - line 67 abstract; figures 1,2	2-15, 17-19
X	US 5 796 735 A (MURTAZA BILAL ET AL) 18 August 1998 (1998-08-18)	1,16
A	column 1, line 49 -column 2, line 54 column 3, line 9 -column 4, line 13 column 4, line 47 -column 5, line 8 abstract; figures 2A-2B,3A-3B	2-15, 17-19

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
22 September 2000	29/09/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Nguyen Xuan Hiep, C

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/06586

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 99 01009 A (NOKIA TELECOMMUNICATIONS OY ;SEPPAENEN JUHA (FI); TUOMISTO JANNE () 7 January 1999 (1999-01-07) page 5, line 15 -page 9, line 12 page 10, line 20 -page 11, line 4 abstract; claims 1,2; figure 6	1,16
A	US 5 845 153 A (SUN CHIH-PING ET AL) 1 December 1998 (1998-12-01) the whole document	1-19

INTERNATIONAL SEARCH REPORT

Information on patent family members

In tional Application No
PCT/US 00/06586

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5742765 A	21-04-1998	NONE	
US 5796735 A	18-08-1998	NONE	
WO 9901009 A	07-01-1999	FI 972800 A AU 7921998 A EP 0995334 A	28-12-1998 19-01-1999 26-04-2000
US 5845153 A	01-12-1998	NONE	